WHAT IS CLAIMED IS:

1. A semiconductor device having a capacitor formed in a multilayer wiring structure, the semiconductor device comprising:

a multilayer wiring structure including a plurality of wiring layers formed on a substrate;

a capacitor arranged in a predetermined wiring layer in the multilayer wiring structure and having a lower electrode, a dielectric film, and an upper electrode;

a first via formed in the predetermined wiring layer and connected to a top surface of the upper electrode of the capacitor; and

a second via formed in an overlying wiring layer stacked on the predetermined wiring layer, the second via being formed on the first via.

2. A semiconductor device according to claim 1, wherein the first via is formed to have a larger cross section than that of the second via.

3. A semiconductor device according to claim 1, wherein the predetermined wiring layer has a third via formed on the lower electrode and a wiring connected to the third via and buried in a surface of the predetermined wiring layer.

4. A semiconductor device according to claim 2, wherein the predetermined wiring layer has a third via formed on the lower electrode and a wiring connected to

the third via and buried in a surface of the predetermined wiring layer.

5. A semiconductor device according to claim 3, wherein the wiring is made of copper, and a copper diffusion stopper film is formed on the surface of the predetermined wiring layer to prevent diffusion of copper forming the wiring.

6. A semiconductor device according to claim 4, wherein the wiring is made of copper, and a copper diffusion stopper film is formed on a surface of the predetermined wiring layer to prevent diffusion of copper forming the wiring.

7. A semiconductor device according to claim 1, wherein the overlying wiring layer has a wiring connected to a top of the second via and buried in a surface of the overlying wiring layer.

8. A semiconductor device according to claim 2, wherein the overlying wiring layer has a wiring connected to a top of the second via and buried in a surface of the overlying wiring layer.

9. A semiconductor device according to claim 1, wherein a third via formed on the lower electrode of the capacitor is provided in the predetermined wiring layer;

a fourth via formed connected to a top of the third via and formed to be thinner than the third via is provided in the overlying wired layer; and

the second and fourth vias are connected to the first and second wirings, respectively, buried in a surface of the overlying wiring layer.

10. A semiconductor device according to claim 2, wherein a third via formed above the lower electrode of the capacitor is provided in the predetermined wiring layer;

a fourth via connected on the third via and formed to be thinner than the third via is provided in the overlying wiring layer; and

the second and fourth vias are connected to the first and second wirings, respectively, buried in a surface of the overlying wiring layer.

11. A semiconductor device according to claim 1, wherein the lower electrode of the capacitor is connected to a wiring buried in a surface of an underlying wiring layer formed under the predetermined wiring layer in which the capacitor is formed.

12. A semiconductor device according to claim 2, wherein the lower electrode of the capacitor is connected to a wiring buried in a surface of an underlying wiring layer formed under the predetermined wiring layer in which the capacitor is formed.

13. A semiconductor device having a capacitor formed in a multilayer wiring structure, the semiconductor device comprising:

at least one impurity diffusion layer formed in a

first area of a semiconductor substrate;

a plurality of wiring layers stacked on the semiconductor substrate and including a first wiring layer having a contact connected to the impurity diffusion layer and a first wiring buried so as to connect to the contact;

a capacitor formed in a predetermined one of the plurality of wiring layers which predetermined wiring layer is formed on a second area different from the first area of the semiconductor substrate, the capacitor having a stacked structure of a lower electrode, a dielectric film, and an upper electrode;

a first via formed on at least the upper electrode in the predetermined wiring layer;

an upper wiring layer having an interlayer insulating film stacked on the predetermined wiring layer, a second via formed in the interlayer insulating film, connected to the first via, and formed to be thinner than the first via, and a second wiring connected to the second via and buried in a surface portion of the upper wiring layer.